Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of constructing an accumulator, comprising:

providing a summing control circuit to produce intermediate result data from initial inputs that are provided to inputs of said summing control circuit, wherein said summing control circuit comprises an adder and control device to perform adds of all layers of said layered tree structure;

providing a left memory bank and a right memory bank;

configuring logic circuits to store said intermediate result data in said left memory bank and in said right memory bank in a manner to simulate a layered tree structure; ~~and~~

configuring said logic circuits to direct said intermediate result data and to direct said initial inputs from an arbitrary length string such that said accumulator maintains the order of operations within each simulated layer;

providing a left source to said adder and control device wherein said left source is selected from among data of said left memory bank and one said initial input; and

providing a right source to said adder and control device wherein said right source is selected from among data of said right memory bank and one said zero value,

wherein said left and right sources are accompanied by control fields which control the flow of data, said control fields including, a cycle type, a routing field and a layer field.

2. (Previously presented) A method according to claim 1 wherein said left memory bank and said right memory bank store every operational layer of said layered tree structure.

3. (Original) A method according to claim 2 wherein said implementing further includes:

segregating said left memory bank into FIFOs, the FIFOs one more than the number of operational layers desired in said layered tree being simulated.

4. (Original) A method according to claim 2 wherein said implementing further includes:

segregating said right memory bank into FIFOs, the FIFOs equal to the number of operational layers desired in said layered tree being simulated.

5 and 6. (Canceled)

7. (Currently amended) A method according to ~~claim 6~~claim 1 wherein said left source and said right source are summed by said adder and control device, the result thereof directed to one of said left memory bank, said right memory bank and a result queue.

8-10. (Canceled)

11. (Currently amended) A method according to ~~claim 10~~claim 1 wherein said control fields of said left source and said right source are combined to assign a single set of control fields to the resulting sum from said adder and control device.

12. (Currently amended) A method according to ~~claim 9~~claim 1 wherein said zero value is selected as said right source if said left source is to pass-through said adder and control device.

13. (Original) A method according to claim 1 wherein said initial input values are floating point in nature.

14. (Currently amended) In an accumulator, a method of operating the accumulator to accumulate initial input values from an arbitrary N-length string, said method simulating a layered tree structure, comprising:

streaming said initial input values in their original order to an input of said accumulator;

selecting a left side source from among a zero value, said initial input values, or a set of intermediate result values;

selecting a right side source from among a zero value, said initial input values or a set of intermediate result values;

adding said left side source and said right side source to generate an adder output value; and

directing said adder output value to one of a memory bank of said accumulator or a result queue of said accumulator, the final result accumulating all N said initial input values, wherein the order of adding is maintained within each said layer,

wherein said streaming comprises:

counting the phase of each initial input;

passing directly without delay those initial inputs having an odd phase count; and

delaying initial inputs having an even phase count, further wherein said delaying is such that said initial inputs having an even phase count are available to be accumulated contemporaneously with said initial inputs having an odd phase count.

15. (Canceled)

16. (Currently amended) A method according to ~~claim 15~~claim 14 further comprising: assigning a set of control fields to each initial input value and to each adder output result value.

17. (Original) A method according to claim 16 wherein assigning includes:

combining said control fields of said left source with the control fields of said right source according to a set of rules, the set of control fields resulting from said combining being assigned to said adder output result value.

18. (Original) A method according to claim 17 wherein said control fields include a cycle type, a routing field and a layer field.

19. (Original) A method according to claim 18 wherein said cycle type is one of a Start, End, Normal and Done types.

20. (Original) A method according to claim 18 further comprising:

partitioning said memory bank into a right memory and left memory bank, each partition representing branches of said layered tree to right and left directions, respectively.

21. (Original) A method according to claim 20 wherein partitioning includes:

segregating said right memory bank into FIFOs, the FIFOs equal to the number of operational layers desired in said layered tree being simulated; and

segregating said left memory bank into FIFOs, the FIFOs one more than the number of operational layers desired in said layered tree being simulated.

22. (Original) A method according to claim 21 wherein said each FIFO of said left memory bank represents one of said operational layers and a bridge layer of said layered tree.

23. (Original) A method according to claim 21 wherein said each FIFO of said left memory bank represents one of said operational layers of said layered tree.

24. (Original) A method according to claim 23 wherein said routing field includes indications of which one of said FIFOs, at each layer, the data that accompanies it belongs.

25. (Original) A method according to claim 23 wherein said left and right source are at the same operational layer when being added except where a bridge layer add is performed.

26. (Original) A method according to claim 25 wherein said length N is allowed to be arbitrarily large by performing bridge layer adds for each of said initial input values exceeding the number allowed by said operational layers.

27. (Original) A method according to claim 14 wherein said initial input values are floating point in nature.

28. (Currently amended) An apparatus configured to simulate a layered tree structure to accumulate initial input values from arbitrary N-length string, comprising:

an input for receiving a stream of said N initial input values;

a left input selector configured to select as a left input one of said initial input values or a left-side intermediate result value from among a plurality of left-side intermediate result values;

a right input selector configured to select as a right input one of said initial input values or a right-side intermediate result value from among a plurality of right-side intermediate result values; ~~and~~

an adder and control device configured to sum together said left input and said right input to produce a sum, said sum being determined to be a left-side intermediate result value, a right-side intermediate result values, or a final output that is representative of the accumulating of said N initial inputs, said adder and control device configured to direct the production of said sum in a manner to maintain the order of adds within each said layer;

a left memory bank configured to store said left-side intermediate result values, wherein the input ports of said memory bank is coupled to said adder and control device, and the output ports of said memory bank are coupled right selection mechanism; and

a right memory bank configured to store said left-side intermediate result values, wherein the input ports of said memory bank is coupled to said adder and control device, and the output ports of said memory bank are coupled to the right selection mechanism.

29. (Canceled)

30. (Currently amended) An apparatus according to ~~claim 29~~claim 28 wherein said memory banks consist of a plurality of FIFOs.

31. (Original) An apparatus according to claim 30 wherein the FIFOs belonging to said left memory bank include a bridge layer FIFO.

32. (Original) An apparatus according to claim 28 further comprising:

a phase counter configured to count said initial input values and configured to output a phase value for each said initial input value.

33. (Original) An apparatus according to claim 32 further comprising:

a delay element coupled to said phase counter and said left input selection mechanism, configured to delay said initial input values that have an even number phase prior to being input to said left selection mechanism.

34. (Original) An apparatus according to claim 28 further comprising a result queue, said result queue to receive from the adder and control device said final output resulting from the accumulating of said N initial inputs.

35. (Original) An apparatus according to claim 31 wherein said left memory bank includes one FIFO for every operational layer in said tree structure.

36. (Original) An apparatus according to claim 35 wherein said right memory bank includes one FIFO for every operational layer in said tree structure.

37. (Previously presented) An apparatus according to claim 28 wherein said initial input values are floating point in nature.